Job Oriented

VLSI DESIGN COURSE

(4 Months)

Contact Us:

Chip Vidhya

1541, 26th Main,26th Cross, 2nd Sector,

H S R layout, Bengaluru – 560 102.

Phone Number: **93807 40137**

Email: **info.chipvidhya@gmail.com**

Website: **www.chipvidhya.com**

Overview

VLSI Design Course where VLSI stands for 'Very Large Scale Integration' which deals the process of designing integrated circuits (ICs) that contain millions or even billions of transistors.
VLSI design course teach students how to design and verify digital circuits. RTL coding, or Register Transfer Level coding, is used to describe the behaviour and functionality of a digital circuit.
An RTL modelling style is a synthesizable coding style. It basically represents the data flow between combinational cloud and registers. RTL Design involves creating a high- level behavioural description of the digital circuit that specifies its functionality, and then translating this description into a register transfer level. The RTL description is then used to synthesize the circuit into a gate-level netlist, which can be used to implement the design in hardware.
The DFT makes the digital circuit testable so that digital design is tested to find it defected or not.

Module 1: Introduction to VLSI

- CMOS Technology
- IC Fabrication Process
- VLSI Design Flow

Module 2: Basic Digital Design

- Number Systems and Codes
- Boolean Algebra and logic gates
- Karnaugh Maps
- Combinational circuits Design
  Adder, Subtractor ,Encoder, Decoder, Multiplexer, Demultiplexer
- Sequential circuit
  Latches flip flop, race around conditions, Registers, counters.
- Registers and Counters.

Module 3: Advanced Digital Design

- Delay in Digital circuit design:
  Combinational circuit delays
  Sequential circuits delays
  Setup and Hold time and its impact on design.
- serial adder, Sequential/random counter design
- Sequence generator ,sequence detector
- Frequency divider
- Finite State Machine: Melay/Moore Model

- FSM Design: pattern detector, vending machine, elevator, product theft detector
- Arbiters
- Glitches and Hazards
- Memory: RAM and Sequential memory.

Module 4: Static Timing Analysis

- Need of Timing Analysis
- Types of Timing Analysis
- Timing Paths
- Delays in Combinational and Sequential Circuits
- Arrival time, Required time and Slack
- Clocks, Clock Slew, Latency, Skew, Jitter
- Setup time and hold time
- Maximum Operating Frequency & Minimum Clock Period
- Derivation of setup and hold timing equation
- Effect of +ve & -ve Clock Skew on Timing Equations
- STA for complex circuits
- Methods of improving Timing

Module 4: RTL coding and Verification using Verilog HDL

- Introduction to Verilog HDL, Language Concepts, Hierarchical modeling Concepts, Abstraction Levels, port connection rules.
- RTL code for Combinational Circuits using Dataflow modeling and verifying the same by writing linear test bench.
- Data Types, operators, Gate-Level modelling and Switch - Level Modeling
- Continuous Assignments, Procedural Blocks, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel blocks, Generate Blocks.
- Delays in continuous concurrent and Procedural assignments.
- RTL code for Combinational Circuits using behavioural modeling and verifying the same by writing task based test bench.
- System tasks, Timescale system tasks and Compiler directives.
- Procedural Continuous Assignment, Overriding Parameters, localparam and conditional compilation execution.
- RTL code for sequential circuits and verifying the same by writing test bench.
- Logic Synthesis with Verilog HDL.
- RTL code for memories and verifying the same by writing test bench.
- Tasks and Functions in Verilog HDL
- Self-checking test bench, Automatic tasks, Named events
- RTL code for FSM and verifying the same by writing test bench.
- Stratified event queue in Verilog HDL

Module 5: Mini project

Module 6: Linux OS

- Introduction to Operating System
- Linux OS and its features
- Layered Architecture of Linux OS
- Linux v/s Windows
- Basic Linux Commands
- Working with VI Editor commands

Module 7: Technology Dependent Synthesis Using DC

- What is Synthesis?
- Logical Synthesis using DC.
- Translation
- Optimization and gate mapping.
- Synthesis Process
- Optimization constraints
- Logical Library
- Targets library and Link library
- Tool flow with example

Module 8: Lint in VLSI design

- What is Lint?
- Need of Lint in ASIC flow
- Lint Check : semantic checks, structural checks, FSM checks
- VC SpyGlass Lint
- LINT flow
- Goals and methodology
- tags and violation report
- Examples

Module 9: Design for Testabilty

- What is testing?
- Need of testing
- What is DFT?
- Role of DFT Engineer
- Types of testing
- Difference between defect and fault
- Fault models: stuck at faults, Stuck open,stuck short(iddq) fault,
- Fault simulation, ATPG,
- Combinational circuit fault detection: path sensitization algorithm.
- Controllability and Observabilty
- DFT techniques: Scan design, EDT IP insertion, Boundary Scan, LBIST, MBIST

Module 10: Major Projects