Job Oriented

VLSI DESIGN AND VERIFICATION COURSE

(6 Months)

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Overview

VLSI Design Course where VLSI full form is the 'Very Large Scale Integration' which covers the process of designing integrated circuits (ICs) that contain millions or even billions of transistors.

VLSI Design involves creating a high- level behavioural description of the digital circuit that specifies its functionality, and then translating this description into a Register Transfer Level (RTL). An RTL modelling style is a synthesizable coding style. It basically represents the data flow between combinational cloud and registers. The RTL description is then used to synthesize the circuit into a gate-level netlist, which can be used to implement the design in hardware.

Design verification is a systematic process that validates and confirms that a design meets its specified requirements and sticking to design guidelines. It is a vital step in the product development cycle, aiming to identify and rectify design issues early on to avoid costly and time-consuming rework during later stages of development. Design verification ensures that the final product, whether it is an integrated circuit (IC), a system-on-chip (SoC), or any electronic system, functions correctly and reliably.

Module 1: Introduction to VLSI

- CMOS Technology
- IC Fabrication Process
- VLSI Design Flow

Module 2: Basic Digital Design

- Number Systems and Codes
- Boolean Algebra and logic gates
- Karnaugh Maps
- Combinational circuits Design
  Adder, Subtractor ,Encoder, Decoder, Multiplexer, Demultiplexer
- Sequential circuit
  Latches flip flop, race around conditions, Registers, counters.
- Registers and Counters.

Module 3: Advanced Digital Design

- Delay in Digital circuit design:
  Combinational circuit delays
  Sequential circuits delays
  Setup and Hold time and its impact on design.
- serial adder, Sequential/random counter design
- Sequence generator ,sequence detector
- Frequency divider

- Finite State Machine: Melay/Moore Model
- FSM Design: pattern detector, vending machine, elevator, product theft detector
- Arbiters
- Glitches and Hazards
- Memory: RAM and Sequential memory.

Module 4: Static Timing Analysis

- Need of Timing Analysis
- Types of Timing Analysis
- Timing Paths
- Delays in Combinational and Sequential Circuits
- Arrival time, Required time and Slack
- Clocks, Clock Slew, Latency, Skew, Jitter
- Setup time and hold time
- Maximum Operating Frequency & Minimum Clock Period
- Derivation of setup and hold timing equation
- Effect of +ve & -ve Clock Skew on Timing Equations
- STA for complex circuits
- Methods of improving Timing

Module 4: RTL coding and Verification using Verilog HDL

- Introduction to Verilog HDL, Language Concepts, Hierarchical modeling Concepts, Abstraction Levels, port connection rules.
- RTL code for Combinational Circuits using Dataflow modeling and verifying the same by writing linear test bench.
- Data Types, operators, Gate-Level modelling and Switch - Level Modeling
- Continuous Assignments, Procedural Blocks, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel blocks, Generate Blocks.
- Delays in continuous concurrent and Procedural assignments.
- RTL code for Combinational Circuits using behavioural modeling and verifying the same by writing task based test bench.
- System tasks, Timescale system tasks and Compiler directives.
- Procedural Continuous Assignment, Overriding Parameters, localparam and conditional compilation execution.
- RTL code for sequential circuits and verifying the same by writing test bench.
- Logic Synthesis with Verilog HDL.
- RTL code for memories and verifying the same by writing test bench.
- Tasks and Functions in Verilog HDL
- Self-checking test bench, Automatic tasks, Named events
- RTL code for FSM and verifying the same by writing test bench.

- Stratified event queue in Verilog HDL

Module 5: Project on Verilog

Module 6: Linux OS

- Introduction to Operating System
- Linux OS and its features
- Layered Architecture of Linux OS
- Linux v/s Windows
- Basic Linux Commands
- Working with VI Editor commands

Module 7: Technology Dependent Synthesis Using DC

- What is Synthesis?
- Logical Synthesis using DC.
- Translation
- Optimization and gate mapping.
- Synthesis Process
- Optimization constraints
- Logical Library
- Targets library and Link library
- Tool flow with example

Module 8: Lint in VLSI design

- What is Lint?
- Need of Lint in ASIC flow
- Lint Check : semantic checks, structural checks, FSM checks
- VC SpyGlass Lint
- LINT flow
- Goals and methodology
- tags and violation report
- Examples

Module 9: System Verilog HVL

- Introduction to Verification
- Introduction to System Verilog
- OOP's Concept
- Randomization & constraint
- Interface & Program block
- IPC
- Building verification environment
- Coverage
- Assertion

Module 10: Major project on System Verilog

Module 11: Universal Verification Methodology (UVM)

- All about UVM
- UVM TB - Building Blocks & their Relationship
- Customized TLM ports in UVM
- Analysis Ports
- OVM Factory
- Sequences
- Coordinated stimulus generation
- UVM Synchronization Mechanisms
- Advanced Messaging
- UVM configuration database

Module 12: Major project on UVM